AMENDMENTS TO CLAIMS

Kindly cancel claim 1 and add claims 2-8 as follows.

1. (Cancel) A logic block in a field programmable gate array, comprising:

a plurality of clusters of logic devices, at least one of said logic devices in each of said plurality of clusters having an input or an output;

a first set of interconnect conductors entering said logic block fro a first side and forming a programmable intersection with said input or said output of said at least one of said logic devices in each of said plurality of clusters;

a second set of interconnect conductors entering said logic block from a second side and forming a programmable intersection with said input of said output of said at least one of said logic devices in each of said plurality of clusters, said first set of interconnect conductors forming a pail-wise hardwired connection with said second set of interconnect conductors; and

an interconnect conductor splitting extension disposed between said first set of interconnect conductors and said second set of interconnect conductors.

2. (New) Circuitry in a field programmable gate array wherein said field programmable gate array includes a logic block having a plurality of clusters wherein each of said plurality of clusters includes a plurality of logic devices wherein at least one of said plurality of logic devices has an input and an output, said circuitry comprising:

a first set of plurality of interconnect conductors entering said logic block from a first side and forming a programmable intersection with said input and said output of said at least one of said plurality of logic devices in each of said plurality of clusters;

a second set of plurality of interconnect conductors entering said logic block from a second direction and forming a first intersection with a set of at least one interconnect conductor of said first set of said plurality of interconnect conductors and forming a second intersection with a second set of a second at least one interconnect conductor of said first set of said plurality of interconnect conductors; and

an interconnect conductor splitting extension disposed between said first intersection and said second intersection formed by said second set of said plurality of interconnect conductors.

3. (New) The circuitry of claim 2 wherein said interconnect conductor splitting extension forms a direct coupling between said first intersection and said second intersection formed by said second set of said plurality of interconnect conductors.

4. (New) The circuitry of claim 2 wherein said interconnect conductor splitting extension further comprises:

a plurality of programmable elements.

5. (New) The circuitry of claim 4 wherein said plurality of programmable elements comprise:

passgates controlled by a plurality static random access memory bits.

6. (New) The circuitry of claim 4 wherein said plurality of programmable elements comprise:

anti-fuses.

7. (New) The circuitry of claim 4 wherein each of said plurality of programmable elements comprises:

a transistor.

8. (New) The circuitry of claim 3 wherein each of said plurality of clusters can be coupled to every other of said plurality of clusters through said interconnect conductor splitting extension.